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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jon M. Huppenthal, Thomas R. Seeman, Lee A. Burton	Confirmation No. 4801
Serial No.: 09/932,330	Art Unit: 2182
Filed: August 17, 2001	Examiner: Sorrell, Eron J.
For: SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT	Customer No. 25235 Docket No. SRC012

DECLARATION OF EVIDENCE UNDER 35 C.F.R. § 1.132

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. § 1.116(e), the attached affidavit is submitted as evidence in support of resolving the pending rejections for U.S. Patent Application Serial No. 09/932,330. Upon assessment of the Examiner's arguments presented in his Final Office Action of April 20, 2006 and the Examiner's response to the Applicant's reply to the Final Office Action in the Advisory Action of July 5, 2006, the Applicants submit this third party evidence regarding technical aspects of the prior art cited against the Applicants. As this case has been submitted for review by the Board of Patent Appeals and Interferences, it is recognized by the Applicants that technical aspects of that disclosed in the reference O'Sullivan, U.S. Patent No. 4,972,457 are at issue. To assist resolving these issues the attached Declaration, prepared by an expert in computer science and computer architecture, is submitted for inclusion in the record.

The Applicants submit that this affidavit is necessary to resolve the issues before the Board and request that this Declaration Under 37 C.F.R. § 1.132 be formally admitted into the record of the aforementioned application.

Date: 11 October 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Jon M. Huppenthal, Thomas R. Seeman, Lee A. Burton

Serial No.: 09/932,330

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For: **SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT**

Confirmation No. 4801

Art Unit: 2182

Examiner: Sorrell, Eron J.

Customer No. 25235

Docket No. SRC012

DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. This Declaration of Evidence is being submitted under 37 C.F.R. § 1.132 to present expert analysis and opinion with respect to the likelihood of success of creating the claimed invention based on the combination of prior art as asserted by the Examiner.

2. I, Wim Bohm, am a Professor of Computer Science at the University of Colorado, Colorado State University campus. I received my PhD in computer science from the University of Utrecht in 1990. I reside at

200 S. Grant Av.
Fort Collins, Co 80521

My CV is attached to this affidavit.

3. I affirm and declare that I have been retained by SRC Computers, Inc. to conduct this analysis and present this opinion, for which I am being compensated regardless of whether my opinion is consistent or inconsistent with the position of the Appellants.

4. I affirm and declare that I have reviewed and analyzed the Examiner's final rejection of U.S. Patent Application Serial No. 09/932,330. I have also reviewed and analyzed the art cited

by the Examiner, namely U.S. Patent No. 6,052,134 by Foster ("Foster") and U.S. Patent No. 4,972,457 by O'Sullivan ("O'Sullivan") in their entirety.

5. I affirm and declare that I have reviewed and analyzed application 09/932,330. In doing so I have identified claims 1, 13 and 25 as the subject of the pending appeal. I declare that my analysis and opinion is based on the computer system described in pending claims 1, 13, and 25 including, but not limited to

> 1. A computer system comprising:
>
> at least one processor;
>
> a controller for coupling said at least one processor to a peripheral bus control block and a memory module bus;
>
> at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus;
>
> at least one memory module slot coupled to said memory module bus; and
>
> a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus.

6. Based on the evidence I have reviewed, it is my expert opinion that it would not be reasonable to expect one skilled in the art, at the time of the Appellants' invention, to be successful in creating the claimed invention by combining the teachings of Foster and O'Sullivan.

7. The computer interface (78) described in O'Sullivan in Column 8, lines 24-30 appears to be a standard serial port interface. One skilled in the art at the time of the Appellants' invention would understand these interfaces to have a Universal Asynchronous Receiver and Transmitter ("UART") as the interface chip. At the time of the Appellants' invention the most common type of UART is the RS-232 protocol. (*Notice that this is an asynchronous, serial interface to an external device.)

8. The RS-232 protocol, which is consistent with the computer interface (78) described in O'Sullivan, was at the time of the Appellants' invention, and remains today, the standard modem

installed in substantially all personal computers ("PCs"). While modems are typically no longer an external component, as is described in O'Sullivan as the hybrid communications control unit, they still use a UART on the main board of the computer.

9. At the time of the Appellants' invention, one skilled in the art would understand that serial or UART based interfaces exist in the Input/Output ("I/O") space of a PC. This space is separate and distinct from the memory space of the PC. The I/O space is used by asynchronous devices associated with the system such as disk drives and modems. Protocols used by such I/O devices are designed to allow the device to interrupt the processor when data or other important events need to be dealt with, thus allowing asynchronous behavior.

10. At the time of the Appellants' invention, one skilled in the art would also understand that in contrast to the I/O space, the memory subsystem of the PC is structured to provide a storage area to the processor that can be accessed very quickly. Thus the protocols used in the memory subsystem are such that the processor/ memory controller is the only device that can issue commands on the memory bus. These commands are very limited typically encompassing only read and write instructions. (*Notice that this is a parallel synchronous interface to an internal storage device.) Thus, one skilled in the art at the time of the Appellants' invention would understand protocols associated with a memory bus or memory expansion slot to be incompatible for use by I/O devices.

11. After careful analysis and consideration of the facts presented to me, my understanding of the invention claimed by the Appellants, in consideration of the art described in Foster and O'Sullivan, and based on my experience and education in the fields of computers science and computing architecture, it is my expert opinion that if one was to take the control unit device, the hybrid communications control unit as described by O'Sullivan, and place it in a memory slot as suggested by the Examiner, one of reasonable skill in the art at the time of the Appellants' invention would not reasonably expect the device or system to function as claimed by the Appellants so as to enable direct data exchange between an external device and the memory bus.

12. To provide a direct data exchange between an external device and the memory bus, as claimed by the Appellants, the O'Sullivan hybrid communication control unit would need to mimic a memory component in the memory bus environment. Memory components provide or receive data from the memory controller when requested. A memory component has no protocol

to asynchronously signal the memory controller that it has data to pass on to the processor. An asynchronous event, as would be consistent with the hybrid communications control unit described in O'Sullivan, would be completely foreign and unrecognizable on the memory bus. Based on these well known restrictions, all of which would be known to one skilled in the art at the time of the Appellants' invention, one skilled in the art would not expect the O'Sullivan device to function so as to enable direct data exchange between an external device and the memory bus.

13. It is also my opinion that one skilled in the art at the time of the Appellants' invention would also not expect the hybrid communication control unit of O'Sullivan to function as described in O'Sullivan when placed in the memory slot. Not only would the hybrid communications control unit fail to enable direct data exchange between an external device and the memory bus, if installed in a memory module slot, it would not be able to act as a communications link between the control bus and any external communications device. From my review and analysis of Foster and O'Sullivan, there does not appear to be any insight or suggestion as to how to proceed to overcome these restrictions.

14. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: October 10, 2006

Wim Bohm

CURRICULUM VITAE A.P.W. BÖHM

Personal Information

Name	**Anton Pedro Willem Böhm**
Birth	July 4, 1948, Rotterdam, Holland
Nationality	Dutch
Marital Status	Married, 1993
Visa Status	Permanent Resident Alien

Qualifications

1984	PhD, University of Utrecht
1974	MSc Mathematics and Computer Science, Technical University Delft

Awards

2004-2005	CSU College of Natural Science Excellence in Undergraduate Teaching Award

Employment

1996 ..	Professor, Computer Science Department, Colorado State University
1990-1996	Associate Professor, Computer Science Department, Colorado State University
1986-1990	Lecturer Computer Science, University of Manchester
1984-1986	Research Fellow, University of Manchester
1978-1984	Research Assistant and Lecturer, University of Utrecht
1974-1978	Research Assistant, Mathematical Centre Amsterdam
1968-1970	Part time Systems Analyst, Unilever Rotterdam
1967-1968	IBM 360 Systems Programmer, Unilever Rotterdam

Current Research Interests

Design and implemtation of a programming languages for fine grain parallel systems, in particular Reconfigurable Computing Systems.

Design of fine-grain-parallel algorithms for image processing, numerical and search applications.

Past Research Activities

Colorado State University. Design and efficient implementation of a strict, functional programming language. Design of parallel functional algorithms.

University of Manchester. Efficient Dataflow Code Generation for SISAL. Parallel simulation of parallel architectures. Distribution of work and data on a multi-processor multi-store dataflow machine.

University of Utrecht. Dataflow analysis. Dataflow computation. Non-determinism. Parallel Algorithms and their complexity.

Mathematical Centre Amsterdam. Portable Compilers for Algol68.

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A.P.W. Böhm, J. van Leeuwen, *Fundamental Theorems in Dataflow Computing*, in Lutz Preis (ed) *Report on the first GTI-workshop*, pp 243-265, University of Paderborn, Germany, 1983.

STATEMENT ON RESEARCH

My approach in research is to combine the study of fundamental issues with practical applications of these. An important fundamental research area is that of machine independent, implicitly parallel programming languages. Some functional or single assignment languages are designed to this goal. These languages have very nice theoretical properties, but it is important to study their efficient implementation and performance, or lack thereof, in order to point out ways to improve them. My current research is in the design of SA-C, a single assignment C language, and its implementation on Reconfigurable Computing Systems. These systems are currently programmed in hardware design languages such as Verilog or VHDL. The aim of my research is to bring the level of abstraction of programming reconfigurable hardware up to that of algorithmic languages and understanding how much, if any, efficiency has been sacrificed. Here are the software projects I have been involved with:

Image Processing on Reconfigurable Systems. For this project I have designed, and our team has implemented SA-C: a high level Image Processing oriented programming language, which is compiled into the configuration codes of (FPGA based) Reconfigurable Systems. We use dataflow code as intermediate form, and have designed a simple abstract machine model for the reconfigurable hardware. The project had four Priciple Investigators: two in Image Processing, one in Programming Language and compilers, and one in system architecture. Also, industry (Khoral Research) is involved to incorporate our system into Khoros, an industry strength programming environment / graphical user interface. The CSU group consisted of twelve people. I managed the compilation and run-time group and was the PI in the last two years of the project.

Functional Numerical Kernels and Applications. With two PhD students I wrote numerical codes, such as FFTs, and Eigensolvers, and Monte Carlo Particle Transport Codes, in a variety of functional programming languages (Id, Haskell, Sisal) to assess their efficiency and expressiveness.

Sisal on Parallel Machines. With two PhD students I designed and implemented a Sisal to shared memory compiler, and a distributed memory compiler.

Fine Grain Multithreaded Code Sisal Compiler. With a group of PhD and MSc students we transformed the Sisal to Manchester dataflow compiler to generate machine independent fine grain multithreaded code.

Multi Processor Dataflow Machine Simulator. From 1987 to 1989 I lead a group of MSc and PhD students at Manchester University to build a multiprocessor dataflow machine simulator.
Sisal to Dataflow Compiler. From 1984 to 1986 I worked at The Manchester University on the design and implementation of the Sisal functional language compiler for the Manchester Dataflow Machine.

Dynamic Networks of Processes. In 1983 I designed and implemented a programming language based on Kahn's simple language for parallelism. A DNP program is a dynamically growing and shrinking network of processes.

Algol 68 Compiler. From 1974 to 1978 I worked in the Algol 68 compiler group at the Mathematical Center (now CWI) in Amsterdam.

SUPERVISION OF RESEARCH STUDENTS

Colorado State University

Masters *A graphical Animation tool for Sisal Programs*, 1990 Khalid Aziz. *The dataflow complexity of algorithms with irregular paralellism*, 1994 Sree Nivarthi. *Towards an Event Simulation and Verification Tool for testing PBX Call Distributors*, 1994 Jim Porter. *Expressiveness and Efficiency of Array Coding Techniques in C++ and Java*, 1997, Preston Appel. *A Host Run Time System for SA-C*, 1999, Harish Kantamneni. *A VHDL Run Time System for Dataflow Execution on Reconfigurable Systems*, 2000, Charlie Ross. *A dataflow graph to VHDL Compiler*, 2000, Monica Chawathe. *SA-C to VHDL Compiler Testing*, 2001, Aparna Shivaswami. *Design and Software Implementation of the SA-C Abstract Hardware Architecture*, 2001, Pankaj Patil. *Scheduling Fixed Point FFT Blocks on FPGAs*, 2001, Pramod Cherukumilli. *Arithmetic Extensions deyond 32 bits in SA-C*, 2001, Mitesh Desai. *Experimental Comparison of Network Performance and Scalabiltity for Windows 2000 and Linux 2.4*, 2001, Alberto Squassabia. *Garbage Elimination in SA-C host code*, 2001, Steve Segreto. *Encryption Algorithms in SA-C*, Madhusudan Kovalmudi, 2003. *A MacroProcessor for the LC-2*, Hari Aiyer, 2004. *Cordic Algorithms in SA-C*, Rama Chitta, 2004. *Horizontal Loop Unrolling in the SA-C Compiler*, Sumanth Kakaraparthi, 2004. **PhD** *Distributed Runtime Support for Task and Data Management*, 1993, Matt Haines. *The Spectrum of Thread Implementations*, 1995, Bhanu Shankar. *Data Dependence Analysis for Functional Array Construction*, 1995, David Garza. *Expressiveness and Efficiency of Declarative Programming Languages*, 1995, Sumit Sur. *Compiling SA-C (Single Assignment C) to Reconfigurable Computing Systems*, 2000, Jeff Hammes.

Manchester University

Masters *Graphics tools for performance monitoring of parallel programs*, 1989, Heidi Tang. *Mapping Problem Classes onto Parallel Computing Systems*, 1988, Mike O'Boyle. *Performance Analysis of a dataflow machine using a multi-ring simulator*, 1987, Yong Meng Teo. **PhD** *Towards a Heterogeneous Dataflow Cluster*, 1990, Yong Meng Teo. *Distributed simulation of a parallel architecture*, 1989, Alvaro Neto.

Utrecht University

Masters *A Syntax (keyword grammar) Driven Programming Environment*, 1983, Pum Walters.

Teaching at Colorado State University

CS153 Introduction to Java. CS200: Algorithms and Data structures. CS253: Programming Languages. CS370: System Software. CS453: Introduction to Compiler Construction. CS453: Programming Languages. CS475: Parallel Programming. CS460: Embedded Systems. CS520: Analysis of Algorithms. CS553: Compilation Techniques. CS575 Parallel algorithms. CS581: Type Systems and Lambda Calculus. CS653: Data Dependence Analysis and Parallel Compilation. CS675: Topics in Parallel Algorithms. CS696: Dataflow Computing.

My philosophy is that we need to teach the students a balance between theory and practice and show them the interaction between the two. At CSU I designed and taught courses in Analysis of Algorithms, Compiler Design, Parallel Programming, Fundamentals of Programming Languages, Embedded Systems, as well as introductory courses on programming, data structures, and programming languages, based on this principle. As is evident from my teaching evaluations, the students are very enthusiastic about my teaching style. I ask a lot of them, but give them responsibility and opportunities to be creative.